REMARKS

Applicants thank the Examiner for the careful and thorough examination of the present application. Applicants have amended independent Claims 1, 19, and 25 to more clearly define the claimed invention over the prior art, and to incorporate the subject matter of former dependent Claims 20 and 26, which have been canceled, into independent Claims 19 and 25, respectively. Applicants have also added new Claims 31-34.

Applicants have amended dependent Claims 2-13, 15-18, 21-24, and 27-30 to address informalities unrelated to the statutory requirements for patentability and to maintain consistency. Applicants have also amended dependent Claim 14 to address an informality helpfully pointed out by the Examiner. Applicants submit that all claims are patentable and present arguments and amendments herein supporting such patentability.

I. The Amended Claims

Amended independent Claim 1 is directed to a semiconductor integrated circuit to execute application code to be received from a memory via external connections. The integrated circuit comprises a processor to execute the application code from the memory, an internal bus to provide the application code to the processor from the memory, and a verifier processor. The verifier processor is to receive the application code via the internal bus. Claim 1 has been amended to recite the verifier processor continually processes the application code using a verification function while the

processor executes the application code from the memory independently of the verifier processor. Support for this amendment may be found on page 3, lines 18-25 of the present application. The verifier processor is also for impairing the function of the integrated circuit in an event that the application code does not satisfy the verification function. The integrated circuit further comprises an instruction monitor to monitor code requests issued by the processor and to impair the function of the integrated circuit unless addresses of the code requests fall within a given range.

Amended independent Claim 19 is similar to Claim 1 and has been similarly amended, but recites the verifier processor processes the application code, and the instruction monitor is connected to the internal bus. Amended independent Claim 25 is directed to a system combination of the semiconductor integrated circuit of Claim 19, and a non-volatile memory that stores application code. New independent Claim 31 is a method counterpart to Claim 1.

II. The Amended Claims Are Patentable

A. The Rejection Over Morais et al.

The Examiner rejected independent Claim 1 over Morais et al. Morais et al. discloses a game console comprising a main CPU 202, a media controller chip 204, a RAM 206 coupled to the media controller chip, and a media communications processor (MCP) 208 coupled to the media controller chip and a ROM 210. (Paragraph 31 & Figure 2A). The MCP includes bootstrap code 212 stored as firmware. The CPU of Morais et al. performs an integrity check on the code

stored in the ROM using the bootstrap code in the MCP. Indeed, the "initialization sequence for the CPU is contained in the bootstrap code." (Paragraph 34).

In contrast, amended independent Claim 1 now recites the processor executes the application code from the memory independently of the verifier processor. The Examiner cited the bootstrap code, stored in the MCP, of Morais et al. as disclosing the verifier processor of the claimed invention, and the CPU of Morais et al. as disclosing the processor of the claimed invention. Since the initialization code of the CPU is contained in the bootstrap code and the CPU performs the integrity check on the ROM code, Applicants submit that Morais et al. fails to disclose the above highlighted recitation.

Moreover, Applicants submit that Morais et al. also fails to disclose an instruction monitor to monitor code requests issued by the processor and to impair the function of the integrated circuit unless addresses of the code requests fall within a given range, as recited by independent Claim 1. Furthermore, none of the cited references makes up for this deficiency of Morais et al. Accordingly, amended independent Claim 1 is patentable over Morais et al.

B. The Rejection Over Warren

The Examiner rejected independent Claim 1, and former dependent Claims 20 and 26 (now amended independent Claims 19 and 25, respectively) over Warren. Warren discloses an integrated circuit comprising a CPU, a bus coupled to the CPU, a memory coupled to the bus, a breakpoint range unit

storing first and second breakpoint addresses, and a logic controller coupled to the breakpoint range unit. The breakpoint range unit compares the instruction address currently being processed by the CPU. If the current instruction address falls within the first and second breakpoint addresses, the breakpoint range unit generates a breakpoint signal, which is received by the logic controller. Upon receipt of the breakpoint signal, the logic controller interrupts the CPU, thereby enabling diagnostic tests on the CPU. (Col. 2, lines 25-47).

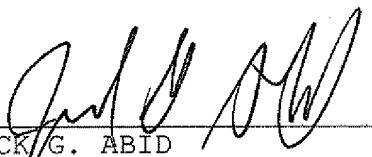
The Examiner contended that the CPU of Warren discloses both the verifier processor and the processor of the claimed invention. Applicants have now amended independent Claims 1, 19, and 25 to recite the processor executes the application code from the memory independently of the verifier processor. The CPU of Warren does not disclose both the processor executing application code independently of the verifier processor, as in the claimed invention. Indeed, the breakpoint range unit of Warren is dependent on the current instruction address from the address store register of the processor. (Col. 2, lines 29, 39-40). Moreover, none of the cited references makes up for this deficiency of Warren.

Accordingly, it is submitted that amended independent Claims 1, 19, and 25 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the amendments to the claims and the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned at the telephone number listed below.

Respectfully submitted,



JACK G. ABID
Reg. No. 58,237
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorney for Applicants